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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/000,036	12/04/2001	Finbar Naven	1267.1028	9313

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EXAMINER	
KUMAR, PANKAJ	

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 08/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/000,036	NAVEN ET AL.	
	Examiner	Art Unit	
	Pankaj Kumar	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-10,15-26,42 and 44* is/are allowed.

6)☒ Claim(s) *11,27 and 35* is/are rejected.

7)☒ Claim(s) *12-14,28-34,36-41 and 43* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/01,11/03,8/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The abstract of the disclosure is objected to because it should not include the title of the invention. Correction is required. See MPEP § 608.01(b).

Claim Objections

2. Claim 11 and it dependent claims are objected to because of the following informalities:

   a. Claim 11 is objected to where it recites "the data stream". It should probably recite 'said stream of serial data'.

3. Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tulpule 4,696,019 in view of Brauns USPN 5,689,533.

6. As per claim 11: Clock recovery circuitry, operable to perform repeating series of N cycles, where N k comprising: N rising-edge latches (Tulpule fig. 2: 32), each connected for receiving stream of serial data (Tulpule fig. 5: shows 32 in detail; 36) and each triggered at a rising edge of a different one of the N cycles (Tulpule col. 17 lines 44-47) of said repeating

series (Tulpule fig. 2a, 11b: clock is repeating) to take a rising-edge sample of the data (Tulpule col. 17 lines 41-44); N falling-edge latches (Tulpule fig. 2: 34), each connected for receiving the data stream (Tulpule fig. 6: shows 34 in detail; 38) and each triggered at a falling edge (Tulpule col. 17 lines 48-53; fig. 6 shows inverting the clock 38 so that the trigger at 3 will occur at the falling edge of 38) of a different one of the N cycles (Tulpule col. 17 lines 40-47: input counter frame, separate counter frame) of said repeating series (Tulpule fig. 2a, 11b: clock is repeating) to take a falling-edge sample of the data (Tulpule col. 17 lines 48-53); and a sample processing circuit which processes the samples (Tulpule fig. 2: elements after 32 and 34 process the samples) to recover a clock signal from the data stream (not in Tulpule but would be obvious as explained below).

7. Tulpule does not teach to recover a clock signal from the data stream. Brauns teaches to recover a clock signal from the data stream (Brauns fig. 1: retimed clock, timing recovery 200, retiming edge; col. 2 lines 9-10). Thus, it would have been obvious, to one of ordinary skill in the art, at time the invention was made, to arrive at the recover a clock signal from the data stream as recited by the instant claims, because the combined teaching of Tulpule with Brauns suggest recover a clock signal from the data stream as recited by the instant claims. Furthermore, one of ordinary skill in the art, would have been motivated to combine the teachings of Tulpule with Brauns because Tulpule suggests clock synchronizing (something broad) in general and Brauns suggests the beneficial use of clock synchronizing by recovering the clock in order to retime with a reference (Brauns col. 1 lines 25-30) in the analogous art of synchronizing.

8. Claim 27, 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Buckner USPN 5,509,037 in view of Eilken USPN 6,445,252.

9. As per claim 27: Data recovery circuitry, for sampling a received serial data stream, comprising: a clock recovery circuit (Buckner col. 2 lines 20-24: retiming) connected for receiving a plurality of candidate clock signals having the same frequency but spaced apart one from the next in phase (Buckner fig. 4: theta1 to theta5), and operable to select, as a recovered clock signal, one of said candidate clock signals that matches said received serial data stream in phase (Buckner col. 2 lines 1-35); an offset clock circuit operable to select, as an offset clock signal, further one of said candidate clock signals different from said candidate clock signal selected as said recovered clock signal; and data sampling circuit operable to sample said received data stream using said offset clock signal (not in Buckner but would be obvious as explained below).

10. Buckner does not teach an offset clock circuit operable to select, as an offset clock signal, further one of said candidate clock signals different from said candidate clock signal selected as said recovered clock signal; and data sampling circuit operable to sample said received data stream using said offset clock signal. Eilken teaches an offset clock circuit operable to select, as an offset clock signal (Eilken col. 9 line 55: "'offset', second recovered output clock signal esclk2"), further one of said candidate clock signals (Eilken col. 9 lines 5-7: first recovered clock signal esclk1) different from said candidate clock signal selected as said recovered clock signal (Eilken: offset, second recovered output clock signal esclk2 is different from first recovered clock signal esclk1); and data sampling circuit operable to sample said received data stream using said offset clock signal (Eilken fig. 3: sampling data ds through PS2 using esclk2). Thus, it

would have been obvious, to one of ordinary skill in the art, at time the invention was made, to arrive at the offset clock circuit operable to select, as an offset clock signal, further one of said candidate clock signals different from said candidate clock signal selected as said recovered clock signal; and data sampling circuit operable to sample said received data stream using said offset clock signal as recited by the instant claims, because the combined teaching of Buckner with Eilken suggest offset clock circuit operable to select, as an offset clock signal, further one of said candidate clock signals different from said candidate clock signal selected as said recovered clock signal; and data sampling circuit operable to sample said received data stream using said offset clock signal as recited by the instant claims. Furthermore, one of ordinary skill in the art, would have been motivated to combine the teachings of Buckner with Eilken because Buckner suggests aligning data with one of the phases of the clock (something broad) in general and Eilken suggests the beneficial use of aligning data with two phases of the clock such as if data is from different places or in knowing which one of the two phases provides better alignment in the analogous art of synchronization.

11. As per claim 35: Circuitry as claimed in claim 27, wherein said candidate clock signals of said plurality are spaced substantially equally in phase one from the next (Buckner fig. 4).

Allowable Subject Matter

12. Claims 12-14, 28-34, 36-41, 43 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

13. Claims 1-10, 15-18, 19-26, 42, 44 are allowed.

14. The following is a statement of reasons for the indication of allowable subject matter: The art of record does not suggest the respective claim combinations together and nor would the respective claim combinations be obvious with:

15. As per claims 1 and its dependent claims (2-10): and a second clocked element connected for receiving said clock signal and said second synchronised signal, and switchable by said clock signal between a responsive state, in which the element is operable response to said state change in said second synchronised signal to change a logic state of third synchronised signal produced thereby, and a non-responsive state in which no state change in the third synchronised signal occurs; wherein, when said clock signal has a first logic state the first clocked element has said non-responsive state and said second clocked element has said responsive state, and when said clock signal has a second logic state the first clocked element has said responsive state and said second clocked element has said non-responsive state.

16. As per claim 15 and its dependent claims (16-18): a second check circuit, connected operatively to the remaining storage elements of the register which form a second set of two or more consecutive storage elements, and producing a second check signal which has first state when any of the storage elements of the second set has said first value and which has a second state when all of the storage elements of the second set have said second value; and a same state detection circuit connected to said first and second check circuits and producing a detection signal, indicating that said control pattern is incorrect, when said first and second check signals have the same state.

17. As per claim 19 and its dependent claims (20-26, 43): a counter connected for receiving said second clock signal and said reset signal and operable, following the change of said reset

signal to said inactive state, to count pulses of said second clock signal and to produce transfer control signals intervals of N cycles of said second clock signal; and a data converter connected for receiving said transfer control signals and said second clock signal, and operable to accept respective first items in response to successive said transfer control signals and to derive said second items from the received first items and to output one of said second items per second-clock-signal cycle.

18. As per claim 42: second check circuit, connected operatively to the remaining storage elements of the register which form a second set of two or more consecutive storage elements, and producing a second check signal which has a first state when any of the storage elements of the second set has said first value and which has second state when all of the storage elements of the second set have said second value; and same state detection circuit connected to said first and second check circuits and producing a detection signal, indicating that said control pattern is incorrect, when said first and second check signals have the same state.

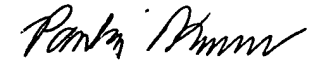
19. As per claim 44: second check means, connected operatively the remaining storage elements of the register which form a second set of two or more consecutive storage elements, for producing a second check signal which has a first state when any of the storage elements of the second set has said first value and which has a second state when all of the storage elements of the second set have said second value; and same state detection means connected to said first and second check means for producing a detection signal, indicating that said control pattern is incorrect, when said first and second check signals have the same state.

Conclusion

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pankaj Kumar whose telephone number is (571) 272-3011. The examiner can normally be reached on Mon, Tues, Thurs and Fri after 8AM to after 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad H. Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Pankaj Kumar
Patent Examiner
Art Unit 2631

PK